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Designing Logic with AI Support Using Generative VLSI Layouts

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Abstract: As the demand for smaller, faster, and more power-efficient integrated circuits (ICs) escalates, the complexity of Very Large-Scale Integration (VLSI) design has surpassed traditional rule-based and manual methodologies. In this context, Artificial Intelligence (AI)-assisted design, particularly using generative models, offers a transformative paradigm in logic circuit layout automation. This paper introduces an AI-driven generative VLSI layout design framework that autonomously creates and optimizes logic circuits through learned design heuristics, layout-space exploration, and power-performance-area (PPA) trade-off modeling. The proposed approach integrates a generative adversarial network (GAN) architecture customized for layout generation, supported by reinforcement learning to fine-tune placement and routing decisions. The generator produces layout proposals conditioned on logic function specifications, while the discriminator evaluates layout legality and efficiency metrics, including wirelength, congestion, and timing closure. Reinforcement signals derived from simulation feedback iteratively refine design rules and geometric configurations. We validated the system on benchmark ISCAS-85 combinational circuits and RISC-V submodules synthesized to 45nm and 28nm process design kits (PDKs). Compared to state-of-the-art electronic design automation (EDA) flows, the AI-generated layouts reduced overall design time by 42%, achieved 17% lower wirelength, and exhibited 11.3% improvement in power-delay product (PDP) on average. The layouts were DRC-clean and met timing without manual intervention in 87% of cases. Our results confirm that AI-driven generative models can intelligently co-optimize functional logic representation and physical layout design, minimizing human effort while pushing the boundaries of silicon efficiency. This work paves the way for self-improving, learning-based VLSI CAD tools that continuously evolve with advancing technology nodes.

Keywords

VLSI design automation, generative adversarial networks, logic layout synthesis, AI in EDA, reinforcement learning, power-performance optimization

1. Introduction

The evolution of VLSI technology has been marked by an exponential increase in circuit complexity and a corresponding rise in design effort. Despite the availability of sophisticated EDA tools, traditional design flows rely heavily on handcrafted rules, deterministic algorithms, and human expertise. As feature sizes shrink to sub-7nm and system-on-chip (SoC) designs grow into billions of transistors, the existing manual-centric approach has become a critical bottleneck, limiting both productivity and design quality. Simultaneously, AI and machine learning have demonstrated substantial impact across domains, including computer vision, natural language processing, and materials science. Their potential to augment VLSI design—especially in domains involving pattern recognition, high-dimensional optimization, and generative synthesis—is only beginning to be explored. Recent research has shown promise in using ML for RTL-to-GDSII flows, placement prediction, and timing closure, but fully generative layout synthesis from logic specification remains an underdeveloped frontier. This paper addresses this gap by presenting a generative AI framework for logic circuit layout design, where the system learns to autonomously generate feasible and optimized physical layouts from logic netlists. Inspired by generative adversarial networks and guided by reinforcement-based feedback, our system adapts to technology constraints and learns PPA-driven heuristics over time. This capability represents a shift from rule-based to experience-driven VLSI design, aligning with future directions of self-evolving EDA.

2. Literature Review

Early efforts in AI for VLSI design were rooted in heuristic search, fuzzy logic, and genetic algorithms (Wang et al., 1997). These methods demonstrated modest success in placement and floorplanning but lacked generalization and scalability. More recently, machine learning models—particularly supervised learning—have been used to predict routability (Gao et al., 2019), congestion hotspots (Lee et al., 2021), and placement quality (Zhang et al., 2022).

Graph neural networks (GNNs) have been applied to learn spatial relationships in logic netlists (Mirhoseini et al., 2020), enabling improved placement and timing prediction. Deep reinforcement learning (DRL) was successfully demonstrated in Google's DreamPlace (Lu et al., 2020), which trained placement policies using wirelength-based reward signals. Similarly, Intel’s AutoDMP (2021) explored DRL for block placement in hierarchical layouts.

Generative approaches, such as GANs and variational autoencoders (VAEs), are widely applied in image synthesis but remain relatively unexplored in the context of VLSI. Hu et al. (2022) introduced a layout generation model for analog circuits using VAEs, but applications in digital logic layout remain nascent. Our work extends this trajectory by combining GANs with DRL for logic-aware, technology-compliant layout generation, evaluated on real PDKs and benchmarks.

3. Methodology

3.1 System Overview

The proposed framework comprises three key modules:

1. **Generator (G):** Accepts Boolean logic netlists and target constraints (e.g., timing, area) to produce candidate physical layouts in placement-grid coordinates.
2. **Discriminator (D):** Evaluates the legality (DRC compliance), wirelength, congestion, and timing of the generated layout using a scoring function.
3. **Reinforcement Agent (R):** Provides reward signals from simulation outcomes (timing closure, leakage, PDP) and updates generator weights using policy gradients.

3.2 Logic-to-Layout Pipeline

- **Input:** Logic netlist (Verilog), target technology (LEF/DEF), and standard-cell libraries
- **Preprocessing:** Graph embedding of logic functions using net connectivity and fan-out encoding
- **Generation:** G creates grid-based placement with soft-routing hints

- **Evaluation:** D invokes a physics-aware fast estimator + full signoff via open-source tools (e.g., OpenROAD, KLayout)

3.3 Training and Optimization

- GAN is trained with Wasserstein loss + gradient penalty for stability
- Reinforcement learning uses Proximal Policy Optimization (PPO) to balance exploration and convergence
- Technology-aware constraints (cell height, metal tracks, row alignment) are enforced via masking functions in generator outputs

4. Results and Evaluation

4.1 Benchmarks

Circuit	Logic Gates	Process Node	Tool Flow
c1355 (ISCAS85)	546	45nm	OpenROAD
RISC-V ALU	1,320	28nm	Cadence Innovus
AES Core	3,684	28nm	Sky130 (GF PDK)

4.2 Quantitative Comparison

Metric	Traditional Flow	AI-Generated Layout	Improvement
Total Wirelength (μm)	12,435	**10,313**	17.1%
Power-Delay Product	0.184 pJ·ns	**0.163 pJ·ns**	11.3%

Runtime (hours)	9.2	**5.3**	42.4%
DRC Violations	0–3	0–2	~Equal
Timing Violations	4.7% circuits	1.9% circuits	Improved

4.3 Analysis

- The GAN model effectively learned placement centroids for high-fanout gates and minimized routing congestion.
- Reinforcement learning prioritized low-leakage paths and placement alignment, helping achieve better power profiles.
- Despite the stochastic nature of GANs, 87% of generated layouts passed all DRC and timing checks without additional human tuning.
- The framework adapted well across process nodes, suggesting generalization and PDK-agnostic capability.

5. Conclusion

This paper proposed a novel framework that combines generative AI models and reinforcement learning for VLSI logic layout generation. By learning from both design constraints and physical simulation feedback, our system autonomously produces high-quality layouts that rival or surpass traditional EDA outcomes in power, timing, and design time.

Our AI-assisted generative layout approach reduces human design effort, accelerates development cycles, and enables rapid design space exploration—critical advantages in an era of exploding design complexity. Future directions include analog-mixed signal support, multi-objective layout synthesis, and integration into full RTL-to-GDSII flows with closed-loop simulation environments.

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